Claims

The following is a copy of Applicant's claims that identifies language being added with underlining ("___") and language being deleted with strikethrough ("———"), as is applicable:

1. (Currently Amended) A method for fabricating micro-electro-mechanical system (MEMS) capacitive resonators, the method comprising:

forming trenches in a substrate;

conformally coating the substrate with an oxide;

filling the coated trenches with polysilicon;

patterning the polysilicon;

releasing a ~~resonator~~ resonating structure derived from the substrate; and

removing the conformally coated oxide.

2. (Original) The method of claim 1, further comprising:

depositing nitride on at least one of an insulating layer and the substrate;

patterning the nitride to isolate pads;

providing polysilicon to the patterned pads; and

metallizing the pads.

3. (Original) The method of claim 1, wherein the releasing comprises separating the resonating structure from the polysilicon.

4. (Original) The method of claim 1, wherein the releasing comprises an isotropic silicon etching of the resonator.

5. (Original) The method of claim 1, wherein the filling includes filling out from sidewalls of the trenches.

6. (Currently Amended) The method of claim 1, wherein the removing includes forming a gap between the ~~resonator~~ resonating structure and the polysilicon in a self-aligned manner.

7. (Original) The method of claim 6, wherein the gap is approximately less than 90 nanometers.

8. (Original) The method of claim 1, wherein the filling includes forming an electrode.

9. (Original) The method of claim 1, wherein the etching includes forming high-aspect ratio trenches.

10-17. (Canceled)

18. (Original) A method for fabricating micro-electro-mechanical system (MEMS) capacitive resonators, the method comprising:

forming trenches in a semiconductor-on-insulator substrate;

conformally coating the semiconductor-on-insulator substrate with an oxide;

filling the coated trenches with polysilicon, wherein electrodes are derived from the polysilicon;

forming release openings; and

removing the conformally coated oxide and an oxide of the semiconductor-on-insulator substrate, wherein a capacitive gap is formed, wherein a resonating element of the capacitive resonator is released.

19. (Original) The method of claim 18, further including:

growing and patterning an insulator oxide, wherein the insulator oxide provides isolation between the semiconductor-on-insulator substrate and wire-bonding pads;

depositing and patterning nitride, wherein the nitride provides protection for the insulator oxide disposed on the pads;

growing and removing a surface treatment oxide, wherein the surface treatment oxide enables the reduction of the roughness of sidewalls of the resonating element;

depositing polysilicon to form the wirebonding pads for drive and sense electrodes;

metallizing the pads; and

patterning the polysilicon inside the trenches.

20. (Original) The method of claim 18, wherein the forming release openings comprises anisotropically etching to an oxide layer of the semiconductor-on-substrate, such that the undercut of the resonating element is facilitated.

21. (Original) The method of claim 18, wherein the filling includes one of filling the trenches with doped LPCVD polysilicon such that the electrodes are formed vertically and depositing and patterning doped LPCVD polysilicon.

22. (Original) The method of claim 18, wherein the forming trenches includes one of deep reactive ion etching and regular reactive ion etching to an oxide layer of the semiconductor-on-insulator substrate.

23. (Original) The method of claim 18, wherein the conformally coating includes depositing a LPCVD high-temperature oxide of approximately less than 100 nanometers.

24. (Original) The method of claim 18, wherein the conformally coating is scalable to correspond to a desired thickness of a lateral gap spacing for the capacitive resonator.

25. (Original) The method of claim 18, wherein the removing comprises an anisotropic plasma etching such that at least a portion of the oxide remains on sidewalls of the resonating element.

26. (Original) The method of claim 18, wherein the releasing comprises exposing the semiconductor-on-insulator substrate to a solution comprising HF:H20 to release the resonating element from a handle layer and the electrodes.

27. (Original) The method of claim 18, wherein the forming trenches includes etching high-aspect ratio trenches.

28. (Original) The method of claim 18, wherein the removing includes forming a gap between the resonating element and the polysilicon in a self-aligned manner.

29-35. (Canceled)

36. (Newly Added) The method of claim 18, wherein the removing is performed to form a plurality of capacitive gaps and release a plurality of resonating elements, each of the plurality of resonating elements electrically isolated from each other.